A/D AND D/A CONVERSION

DIGITAL –TO–ANALOG CONVERSION

The Digital-to-Analog Converter is a device that convert a binary code to an analog signal, the input code word typically a 2's compliment number. It is typically designated as a DAC, D/A, or D-to-A. The input-output function depicting the output voltage produced as a function of the binary code is shown in Figure 4-1.

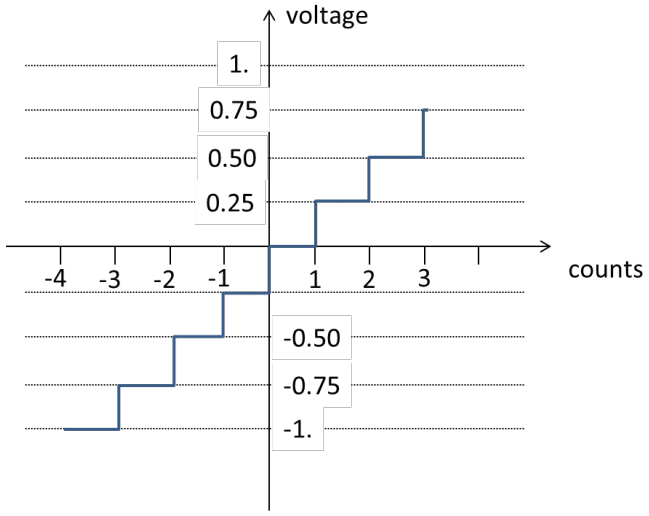


Figure 4-1 – D/A Conversion function: a 3 bit DAC and the 2's compliment input codes

In this figure note that the output voltage does not reach a voltage of 1. The largest positive integer for a 3 bit 2's compliment number is 3, and at the other end -4. The additional unreachable step in this converter that has a "maximum" voltage of +1 has little effect on converters with a larger number of bits. Creating the output function in this way avoids a non-zero output voltage for an input count value of 0. For this converter the maximum and minimum voltages are $V_{max} = 1$ and $V_{min} = -1$.

Consider the following 2 bit unipolar DAC whose output voltage function is shown in Figure 4-2.

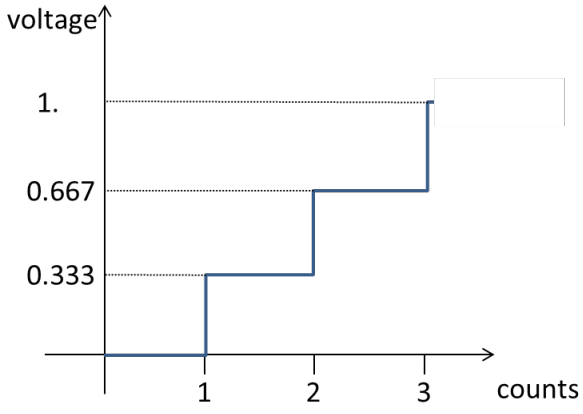


Figure 4-2 – D/A Conversion function: a 2 bit unipolar DAC and positive input codes

For this converter the maximum and minimum voltages are $V_{max} = 1$ and $V_{min} = 0$.

For an N bit converter which permits M = 2^N binary codes, there are M-1 output transitions. The full scale range V_F is the total range of possible output voltages: V_{max} - V_{min}. The voltage resolution V_R is computed as follows:

$$V_R = \frac{V_F}{M-1} \qquad \text{or} \qquad V_R = \frac{V_F}{M}$$

It is the first when the output range is unipolar and the 2nd when bipolar.

DAC Example 1 – Output resolution: A 16 bit unipolar DAC has a full scale voltage ranging from 0 to 10 volt. What is the output resolution?

Solution –

$$V_R = \frac{10}{2^{16}-1} = \frac{10}{65535} = 0.00015259 \text{ volts / count}$$

The error sources affecting the DAC output accuracy include:

- clock jitter
- sample domain voltage error
- quantization

A simulation model is readily constructed that includes all but clock jitter. It is given in Figure 4-3. To the output binary code, which has units of counts, the sample domain error is added at that same sample rate to represent any output voltage error that is held over the sample interval. This is converted from counts to volts with the resolution conversion factor V_R .

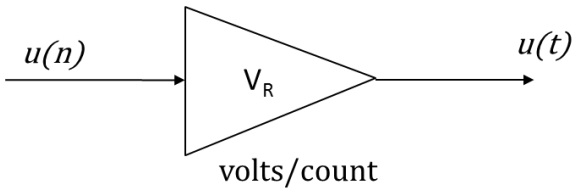


Figure 4-3 – Simulink model of a DAC: note that the output time domain signal is simply the recognition that Simulink holds discrete samples over the time they are inputs to any downstream continuous-time processes.

DAC Example 2 – A D/A with a range of ±10 V is employed in an application requiring a resolution of 0.01 V. What is the number of bits required?

Solution –

$$V_R = \frac{V_F}{2^N} = \frac{20}{2^N} \le 0.01$$

$$2^N \ge 2000$$

Thus the number of bits N must be 11. With an 11 bit converter and a full scale range of 20 volts the resulting resolution will be

$$V_R = \frac{20}{2048} = 0.009765625 \text{ volts}$$

DAC Example 3 – A DAC with a range of ±15 V is employed in an application requiring a resolution of 0.001 V. What is the number of bits required?

Solution –

$$V_R = \frac{30}{2^N} \le 0.001$$

The required number of bits satisfying this requirement is computed to be 15 bits: $\frac{30}{2^{15}} = 0.0009155$ volts.

DAC Example 4 – A DAC is to be used to produce a velocity command voltage to drive a motor over a range of speeds ranging from 0 to 3000 degrees/second. The resolution of the velocity command must be sufficient to provide 1°/second steps or less. How many bits are required and what is the resolution of the DAC in volts?

Solution – The DAC must be able to produce 3001 voltage amplitude levels or more. The closest power of 2 exceeding 3001 is 4096 = 2^12. Thus 12 bits are needed. The resulting resolution will be

$$\text{Speed resolution} = \frac{3000}{2^{12}-1} = 0.7326 \frac{(\text{degrees/ second})}{\text{count}}$$

DAC Example 5 – Assuming the DAC is bipolar, how many bits are required to produce a voltage signal with a resolution of (a) 0.001%, (b) 0.1%, (c) 1%, and (d) 10 %?

Solution – The resolution given as a percentage of full scale is equal to the resolution voltage divided by the full scale voltage, scaled up by 100:

$$100\frac{V_R}{V_F} = 100\frac{1}{2^N}$$

(a) For an accuracy of .001% or better: $\frac{100}{2^N} < 0.001$ or equivalently $2^N > 100,000$; so the answer is $N = 17$ bits. (b) For 0.1%, $2^N > 1000$, and $N = 10$ bits, (c) for 1%, $2^N > 100$, and $N = 8$ bits, and (d) for 10%, $2^N > 10$, and $N = 4$ bits.

DAC Example 6 – A 6 bit, unipolar, 0 to 1 volt DAC receives the following 2's compliment, binary codes. Determine the voltage output levels (assuming a noiseless, DAC that is error free other than quantization)

Solution – The voltage resolution is $V_R = \frac{V_F}{2^N - 1} = \frac{1}{2^6 - 1} = 0.015873$ volts. At 1 count the output will be 0.015873 volts. For other counts values it will scale proportionally.

Input counts	Output volts
0	0
1	0.01587
10	0.15873
30	0.47619
63	1.00000

DAC Example 7 – Tx spectrum – sinusoid at 500 Hz, T = 1/4000 – A DAC running at 4 kHz is receiving samples from a 507.8125 Hz sinusoid. For this analysis assume that the DAC output range is ±1 V and that the DAC has infinite resolution (i.e. no quantization). Compute the output spectrum using an 8192 sample FFT sampling the DAC output voltage at 40 kHz. Scale the output of the FFT by (2/N), scaling it consistently to signal amplitude. Compare the spectrum to the spectral line component levels expected based upon the analysis of the Signal Reconstruction section above.

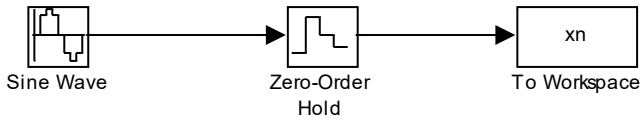
Solution – Begin by computing the expected levels based on the formula $|H(f)| = \dfrac{\sin(\pi fT)}{\pi fT}$. At 507.8 Hz we have $|H(507.8)| \approx \dfrac{\sin(\pi/8)}{\pi/8} = 0.97$. At the spectral images around 4000 Hz we have two components, at 4000±508 Hz:

$$|H(f)| = \frac{\sin(\pi 3492/4000)}{\pi 3492/4000} = 0.14 \qquad |H(f)| = \left|\frac{\sin(\pi 4508/4000)}{\pi 4508/4000}\right| = 0.11$$

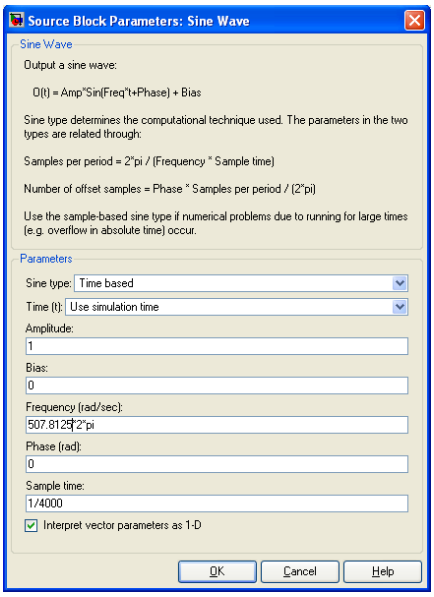
At the spectral images at 7500 and 8500 we have:

$$|H(f)| = \left|\frac{\sin(\pi 7492/4000)}{\pi 7492/4000}\right| = 0.065 \qquad |H(f)| = \left|\frac{\sin(\pi 8508/4000)}{\pi 8508/4000}\right| = 0.057$$

Create the following Simulink model:



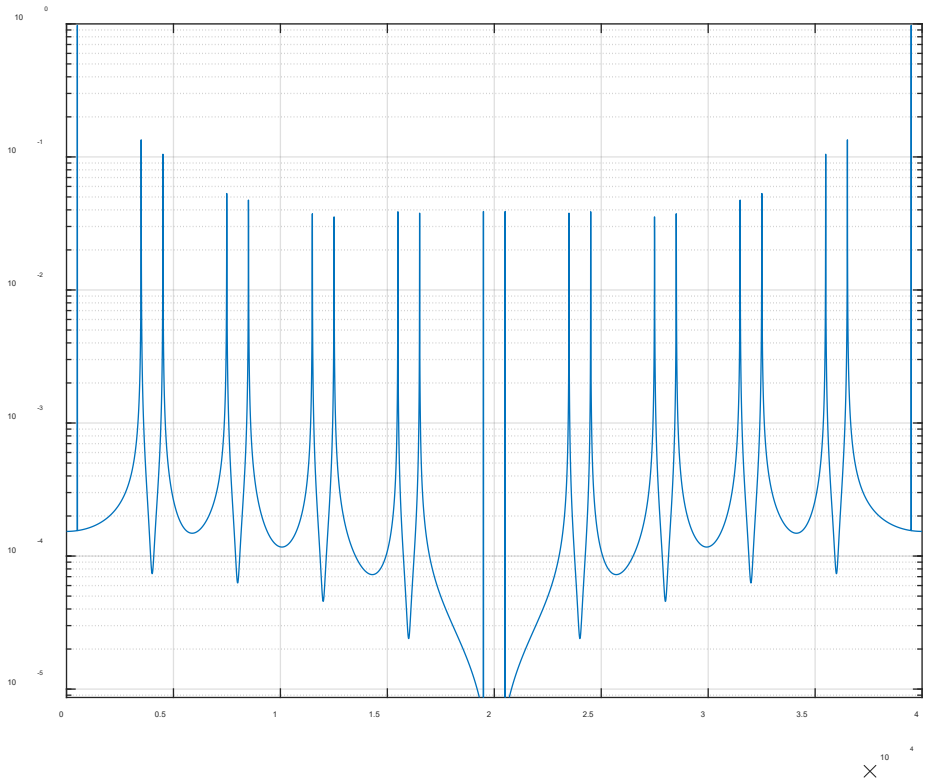
with sampling time 1/40000. Run it for 0.25 seconds, producing 10,000 samples in workspace variable xn.



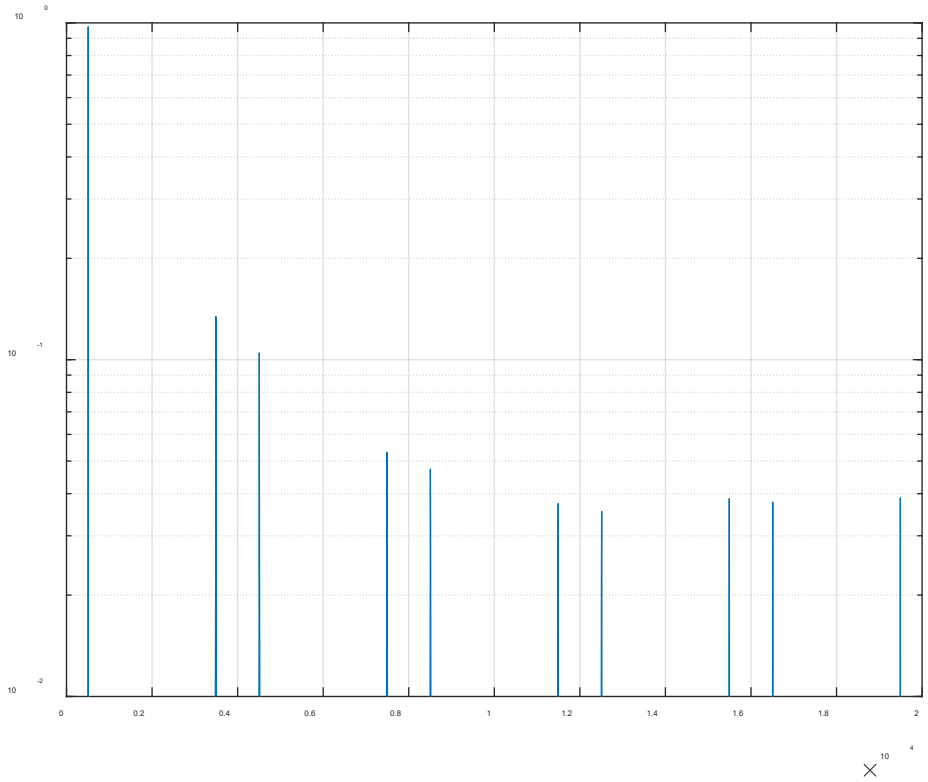
And process the data with the following:

```
X = fft(xn(1:8192));
absX = abs(X);
df = 40000/8192;
f = (0:1:8191)*df;
semilogy(f,absX*2/(8192))
grid
axis([0 20000 0.01 1])
```

The spectrum plotted initially without scaling (the last line above was not applied):



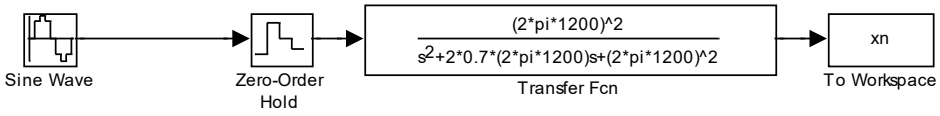
Zooming in to see the first 5 peaks that we're interested in:



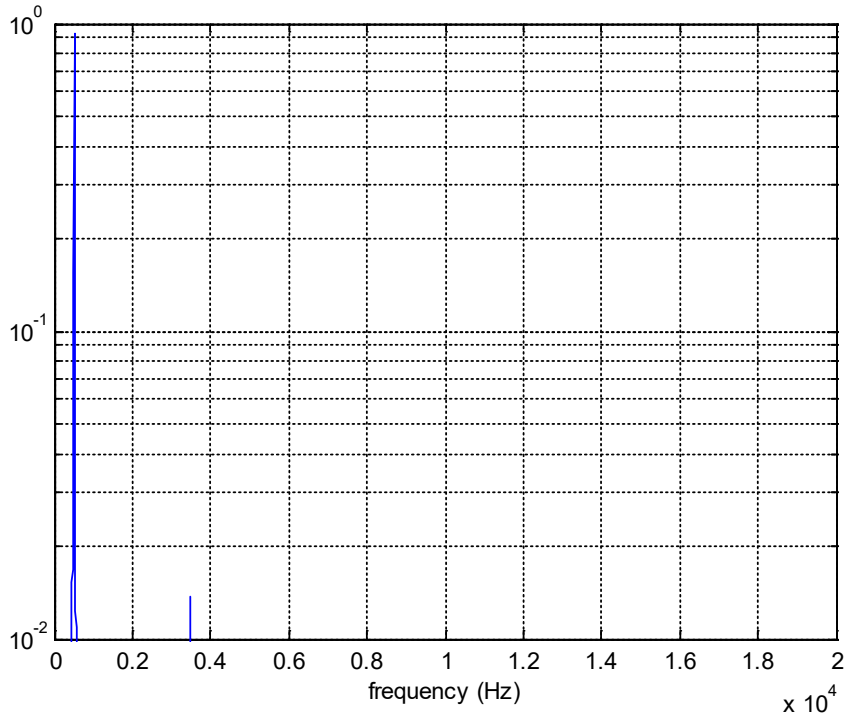
It can readily be verified that the signal spectral lines at the imaged locations approximately have the expected amplitudes.

DAC Example 8 – Tx spectrum of Example 7 with a low pass reconstruction filter, BW = 1200 Hz: Add a 2nd order low pass filter with a break frequency of 1200 Hz and recomputed the signal spectrum. How much is the signal component at approximately 3500 Hz reduced?

Solution – To the model we add the 2nd order filter:



which is processed with the m-code above, yielding:

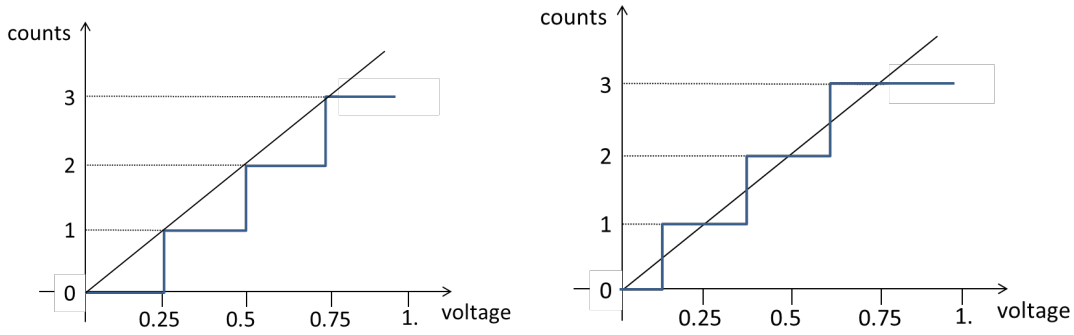


The signal component near 3500 Hz is reduced from 0.14 to 0.04 in amplitude.

ANALOG–TO–DIGITAL CONVERSION

An Analog-to-Digital Converter is a device that receives an analog input voltage and outputs a binary representation of that voltage, repeating this process at the regular time interval called the sampling rate, hence the name given to the output -- a sample. There are two principle performance parameters associated with the ADCs – sampling rate and quantization. These parameters define resolution of the device in time and signal amplitude dimensions. Both are important to the system designer, the sampling rate defining an upper bound on the signal bandwidth that can be represented in the digital domain, and the quantization defining a lower bound on the error associated with the signal being sampled. Selection of these parameters for particular applications is therefore a critical design choice; there selection is discussed below. Other errors sources impacting ADC performance particularly in higher speed ADC's is the internal analog noise.

The ADC will convert an analog input voltage in accordance with a quantization function like that of Figure 4-4.



(a) (b)

Figure 4-4 – ADC Converter conversion function -- quantization errors Q equaling in (a) the resolution, and (b) the resolution*0.5.

Note that the quantization error Q in (a) is V_R and in (b) is $V_R/2$. The ADC resolution is given by

$$V_R = \frac{V_F}{2^N}$$

with V_F the voltage full scale range.

A/D conversion model -- the ADC conversion model is the sampling model depicted in Figure 4-5 followed by the two noted error sources, additive internal Gaussian noise and quantization. This sampling model produces from the continuous signal *y(t)* digital samples *y(n),* converting from the time domain continuous-time signal to digital samples with the C/D function block (continuous to discrete). This model is converted to an equivalent Simulink model in Figure 4-6. The Gaussian noise adds to the digital samples with a noise samples defined by the variance of the Gaussian probability density function. Both the input samples *y(n)* and the noise samples *η(n)* are real numbers and have not yet been quantized. That occurs by scaling by the resolution and either rounding or flooring.

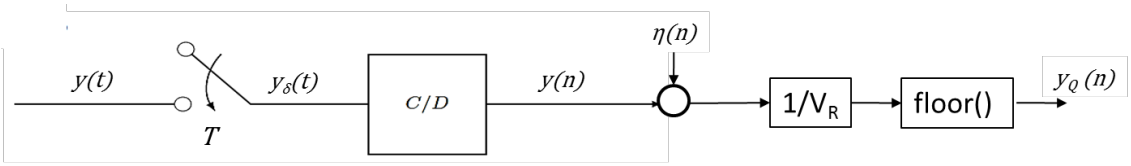


Figure 4-5 – ADC Converter model block diagram – a C/D conversion plus internal noise and quantization

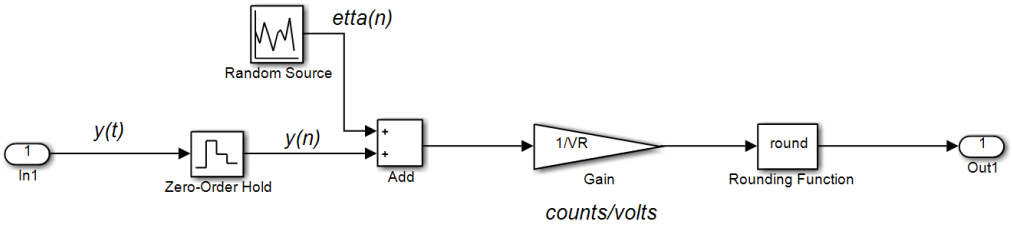


Figure 4-6 – ADC Converter model Simulink block diagram – a S/H block plus internal noise and quantization

ADC Example 1 – Quantization computation: An A/D converter has a full scale input range of 0 to 10 volts. It is a 12 bit converter. What is the voltage resolution?

Solution – The number of quantization levels = $2^{12} = 4096$. The output values run from 0 to 4095.

- The design will reach the effective value of 4096 at 10 volts, thus there are 4096 quantization intervals and the resolution is:
  - 10/4096 = 0.0024414 volts

ADC Example 2 -- A submarine depth sensor with an analog voltage output is sampled by an ADC. The output voltage varies linearly from 0 to 7 volts as the depth varies from 0 to 1,000 feet. The allowable error due to quantization is 4 feet.

How many bits are required (assuming the round method) to provide a quantization error of no more than 4 feet?

How many bits are required to provide a quantization error of no more than ½ a foot?

Solution – A maximum error of 4 feet with the rounding method occurs when the quantization level is 8 feet. Quantization of 8 feet over a 1000 foot full scale range determines the

$$\text{Depth Resolution} = \frac{V_F}{2^N} = \frac{1000}{2^N} \le 8 \quad \text{feet}$$

This is achieved with a 7 bit converter. The resulting quantization level is 1000/2^7 = 7.8 feet

For a 0.5 foot maximum error, we have $\frac{V_F}{2^N} = \frac{1000}{2^N} \le 1$ foot, requiring $N = 10$ bits.

ADC Example 3 – Simulink model example: Construct a Simulink model of an ADC having a clock rate of 10kH, 8 bits of resolution, a full scale range of ±5 volts, and internal noise with a standard deviation of 0.5Q where Q is a quantization step; i.e. equal to the resolution. Input samples generated at 10 kHz are produced by a sinusoid with a frequency 996.1 Hz and amplitude of 4 volts. Run this for 200 msec with and without the random noise. Plot the amplitude spectrum for both cases.

Solution – Computing first the resolution in volts:

$$V_R = \frac{V_F}{2^N} = \frac{10}{2^8} = 0.039 \text{ volts}$$

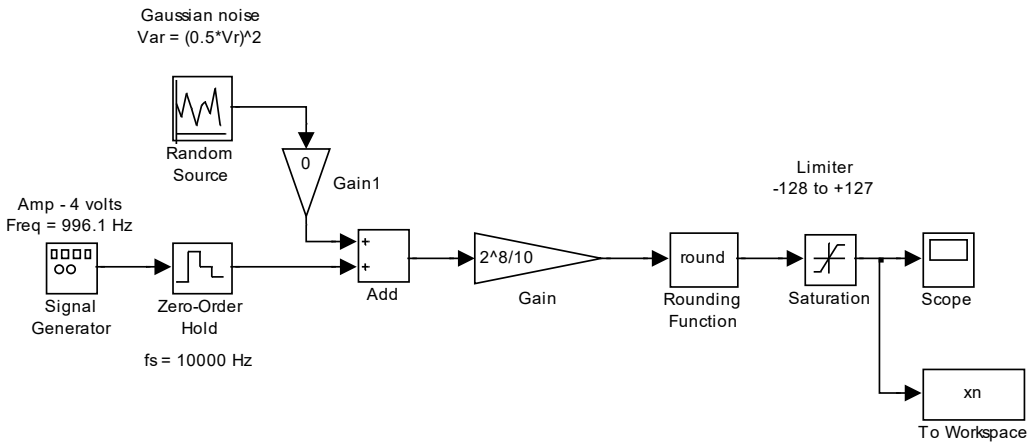
A random source with a 10000 Hz sample frequency is created with a variance $(0.5*0.039)^2$. The Signal Generator produces the 1000 Hz, 4 volt amplitude sinusoid. Dividing this analog sum with a gain block converts to counts. Round to integerize and limit to set the full-scale range. For an 8 bit ADC the output range is -128 to +127 counts.

The following model was constructed, with a gain on the random noise to turn it off or on.

```
xn=squeeze(xn);

X = fft(xn(1:1024));

absX = abs(X);
```



There are two sources of noise, quantizaton noise resulting in the amplitude spectrum directly below, and internal ADC noise of variance $(V_R/2)^2$, shown as the 2nd spectrum.